Module 12: **Design of CMOS logic gates using transistors**

Learning objectives:

Study of the following topics -

Digital logic gates

CMOS inverter

CMOS NAND gate

CMOS NOR gate

CMOS AND and OR gates

This module is concerned with the design of basic logic gates in CMOS technology. The basics of logic gates are discussed as an introduction. This is followed by discussion on CMOS inverter in terms of its basic structure and switching characteristics. CMOS NAND, NOR, AND and OR gates are described next.

First go through the Powerpoint slides and the videos and then complete the associated reading assignments for this module.

Reading assignments

Read the following Wikipedia article:

<http://en.wikipedia.org/wiki/Inverter_(logic_gate)>

Questions

Q1. The power dissipated by a CMOS inveter is given by ½ CV2f. Here C is the capacitance of the inverter’s input, V is the supply voltage and f is the operating frequency. Given a circuit with 100 inverters (or inverter equivalent CMOS logic gates), operating at 5 volts supply voltage and 10 MHz clock frequency, calculate its electrical power dissipation. Take the capacitance of each inverter input as 2 femto Farad (2x10-15 Farad).